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National Semiconductor

August 2000

LM4765 *Overture*™ Audio Power Amplifier Series Dual 30W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM4765 is a stereo audio amplifier capable of delivering typically 30W per channel of continuous average output power into an 8Ω load with less than 0.1% THD+N.

Each amplifier has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM4765, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1kHz at 2 x 25W continuous average output power into 8Ω: 0.1% (max)
- THD+N at 1kHz at continuous average output power of 2 x 30W into 8Ω: 0.009% (typ)
- Standby current: 6.5mA (typ)

Features

- SPiKe Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute mode
- Standby-mode
- Non-Isolated 15-lead TO-220 package
- Wide supply range 20V - 66V

Applications

- High-end stereo TVs
- Component stereo
- Compact stereo

Typical Application

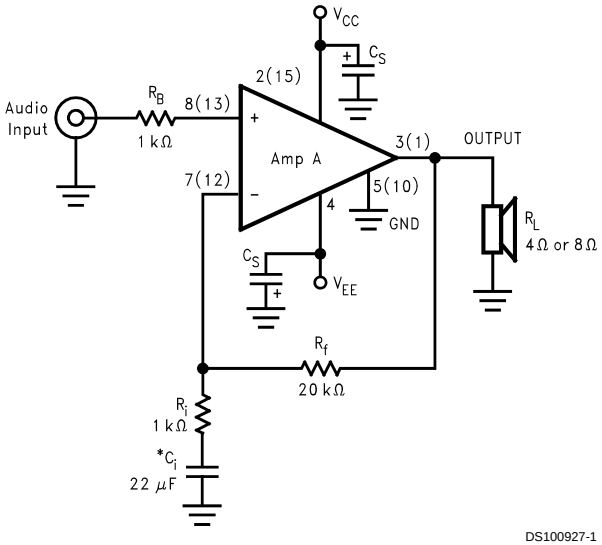


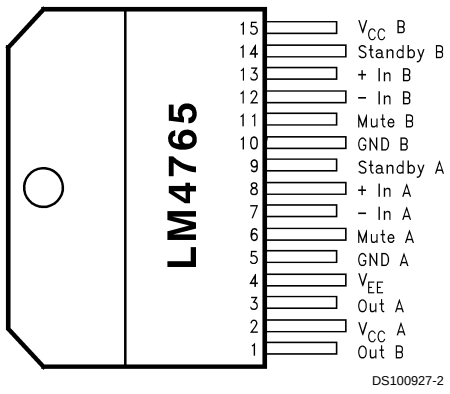
FIGURE 1. Typical Audio Amplifier Application Circuit

Note: Numbers in parentheses represent pinout for amplifier B.

*Optional component dependent upon specific design requirements.

Connection Diagram

Plastic Package



Top View
Non-Isolated Package
Order Number LM4765T
See NS Package Number TA15A

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Absolute Maximum Ratings (Notes 5, 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $\|V_{CC}\| + \|V_{EE}\|$ (No Input)	66V
Supply Voltage $\|V_{CC}\| + \|V_{EE}\|$ (with Input)	64V
Common Mode Input Voltage	(V_{CC} or V_{EE}) and $\|V_{CC}\| + \|V_{EE}\| \leq 60V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 6)	62.5W
ESD Susceptability (Note 7)	2000V
Junction Temperature (Note 8)	150˚C
Thermal Resistance	
Non-Isolated T-Package	
θ_{JC}	1˚C/W
Soldering Information	
T Package (10 sec.)	260˚C
Storage Temperature	−40˚C to +150˚C

Operating Ratings (Notes 4, 5)

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-20˚C \leq T_A \leq +85˚C$
Supply Voltage $\|V_{CC}\| + \|V_{EE}\|$(Note 1)	20V to 64V

Electrical Characteristics (Notes 4, 5)

The following specifications apply for V_{CC} = +28V, V_{EE} = −28V with R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4765		Units (Limits)
			Typical (Note 9)	Limit (Note 10)	
$\|V_{CC}\| + \|V_{EE}\|$	Power Supply Voltage (Note 11)	GND − $V_{EE} \geq$ 9V	18	20 64	V (min) V (max)
P_O (Note 3)	Output Power (Continuous Average)	THD + N = 0.1% (max), f = 1 kHz			
		$\|V_{CC}\| = \|V_{EE}\|$ = 28V, R_L = 8Ω	30	25	W/ch (min)
		$\|V_{CC}\| = \|V_{EE}\|$ = 20V, R_L = 4Ω	22	15	W/ch (min)
THD + N	Total Harmonic Distortion Plus Noise	30 W/ch, R_L = 8Ω	0.08		%
		15 W/ch, R_L = 4Ω, $\|V_{CC}\| = \|V_{EE}\|$ = 20V	0.1		%
		20 Hz ≤ f ≤ 20 kHz, A_V = 26 dB			
X_{talk}	Channel Separation	f = 1 kHz, V_O = 10.9 Vrms	80		dB
SR (Note 3)	Slew Rate	V_{IN} = 1.414 Vrms, t_{rise} = 2 ns	18	12	V/µs (min)
I_{total} (Note 2)	Total Quiescent Power Supply Current	Both Amplifiers V_{CM} = 0V, V_O = 0V, I_O = 0 mA			
		Standby: Off	50	80	mA (max)
		Standby: On	6.5	8	mA (max)
V_{OS} (Note 2)	Input Offset Voltage	V_{CM} = 0V, I_O = 0 mA	2.0	15	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O = 0 mA	0.2	0.5	µA (max)
I_{OS}	Input Offset Current	V_{CM} = 0V, I_O = 0 mA	0.002	0.2	µA (max)
I_O	Output Current Limit	$\|V_{CC}\| = \|V_{EE}\|$ = 10V, t_{ON} = 10 ms, V_O = 0V	3.5	2.9	Apk (min)
V_{OD} (Note 2)	Output Dropout Voltage (Note 12)	$\|V_{CC}–V_O\|$, V_{CC} = 20V, I_O = +100 mA	1.8	2.3	V (max)
		$\|V_O–V_{EE}\|$, V_{EE} = −20V, I_O = −100 mA	2.5	3.2	V (max)
PSRR (Note 2)	Power Supply Rejection Ratio	V_{CC} = 30V to 10V, V_{EE} = −30V, V_{CM} = 0V, I_O = 0 mA	115	85	dB (min)
		V_{CC} = 30V, V_{EE} = −30V to −10V V_{CM} = 0V, I_O = 0 mA	110	85	dB (min)
CMRR (Note 2)	Common Mode Rejection Ratio	V_{CC} = 35V to 10V, V_{EE} = −10V to −35V, V_{CM} = 10V to −10V, I_O = 0 mA	110	80	dB (min)
A_{VOL} (Note 2)	Open Loop Voltage Gain	R_L = 2 kΩ, Δ V_O = 30V	110	90	dB (min)

Electrical Characteristics (Notes 4, 5) (Continued)

The following specifications apply for V_{CC} = +28V, V_{EE} = −28V with R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4765		Units (Limits)
			Typical (Note 9)	Limit (Note 10)	
GBWP	Gain Bandwidth Product	f_O = 100 kHz, V_{IN} = 50 mVrms	7.5	5	MHz (min)
e_{IN} (Note 3)	Input Noise	IHF—A Weighting Filter R_{IN} = 600Ω (Input Referred)	2.0	8	µV (max)
SNR	Signal-to-Noise Ratio	P_O = 1W, A—Weighted, Measured at 1 kHz, R_S = 25Ω P_O = 25W, A—Weighted Measured at 1 kHz, R_S = 25Ω	98 108		dB dB
A_M	Mute Attenuation	Pin 6,11 at 2.5V	115	80	dB (min)
Standby Pin					
V_{IL}	Standby Low Input Voltage	Not in Standby Mode		0.8	V (max)
V_{IH}	Standby High Input Voltage	In Standby Mode	2.0	2.5	V (min)
Mute pin					
V_{IL}	Mute Low Input Voltage	Outputs Not Muted		0.8	V (max)
V_{IH}	Mute High Input Voltage	Outputs Muted	2.0	2.5	V (min)

Note 1: Operation is guaranteed up to 64V, however, distortion may be introduced from **SPiKe** Protection Circuitry if proper thermal considerations are not taken into account. Refer to the Application Information section for a complete explanation.

Note 2: DC Electrical Test; Refer to Test Circuit #1.

Note 3: AC Electrical Test; Refer to Test Circuit #2.

Note 4: All voltages are measured with respect to the GND pins (5, 10), unless otherwise specified.

Note 5: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 6: For operating at case temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and a thermal resistance of θ_{JC} = 1˚C/W for the T package. Refer to the section Determining the Correct Heat Sink in the Application Information section.

Note 7: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 8: The operating junction temperature maximum is 150˚C, however, the instantaneous Safe Operating Area temperature is 250˚C.

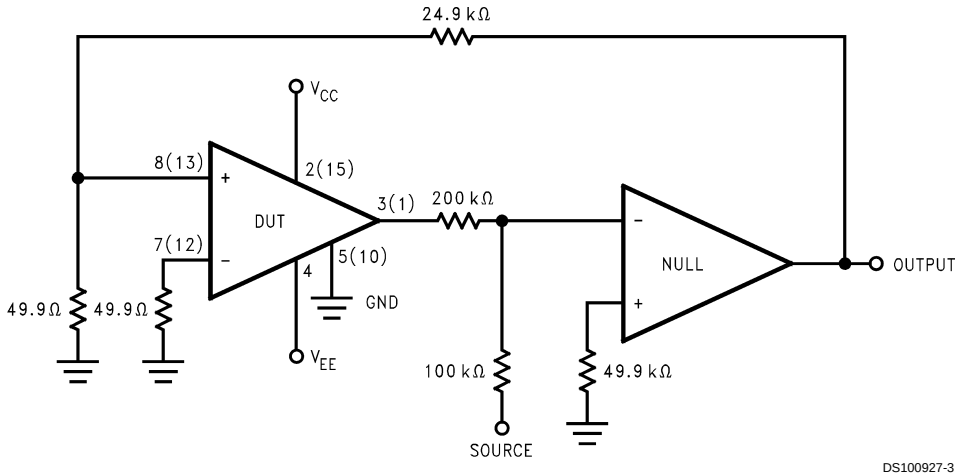
Note 9: Typicals are measured at 25˚C and represent the parametric norm.

Note 10: Limits are guarantees that all parts are tested in production to meet the stated values.

Note 11: V_{EE} must have at least −9V at its pin with reference to ground in order for the under-voltage protection circuitry to be disabled. In addition, the voltage differential between V_{CC} and V_{EE} must be greater than 14V.

Note 12: The output dropout voltage, V_{OD}, is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the Typical Performance Characteristics section.

Test Circuit #1 (Note 2) (DC Electrical Test Circuit)



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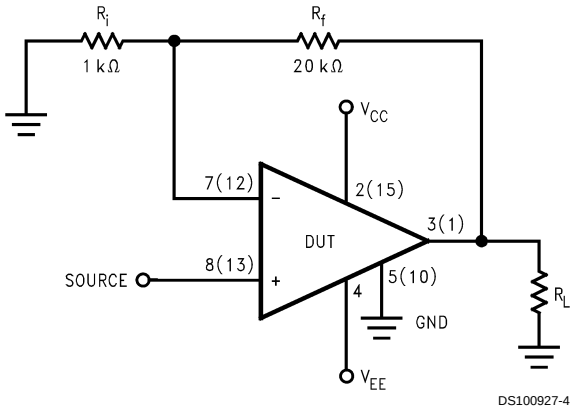
Test Circuit #2 (Note 3) (AC Electrical Test Circuit)



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Bridged Amplifier Application Circuit

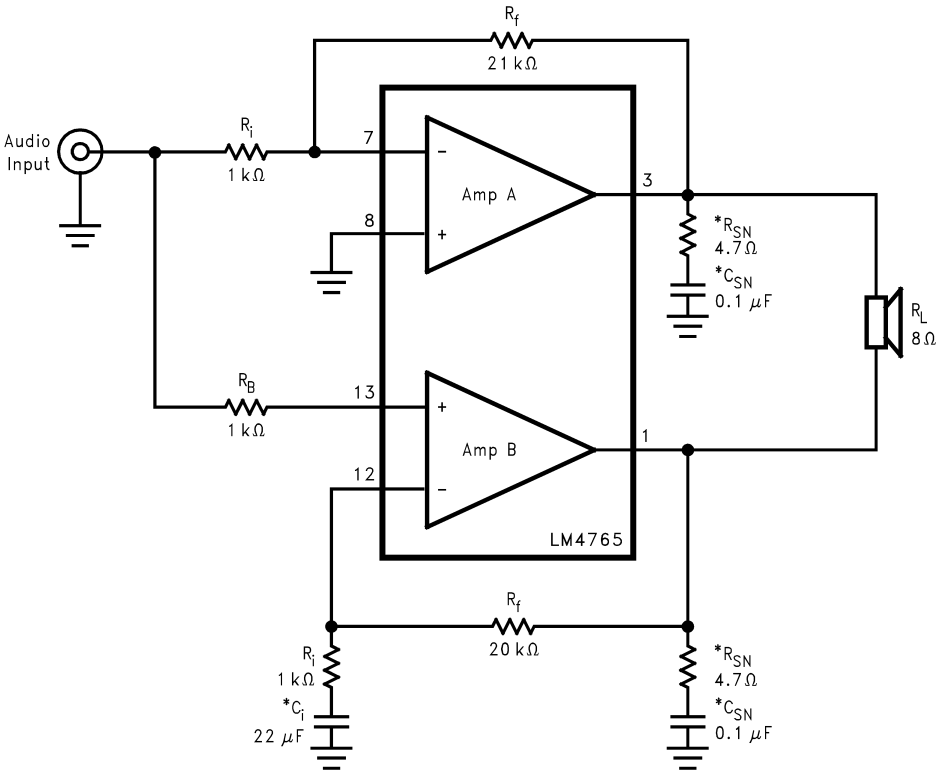


FIGURE 2. Bridged Amplifier Application Circuit

Single Supply Application Circuit

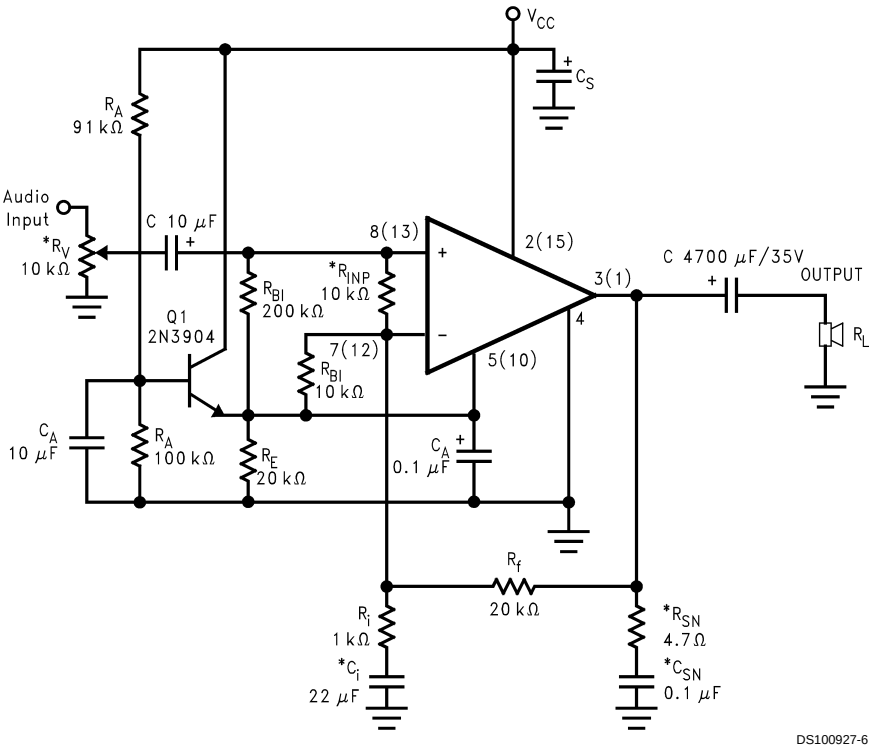


FIGURE 3. Single Supply Amplifier Application Circuit

Note: *Optional components dependent upon specific design requirements.

Auxiliary Amplifier Application Circuit

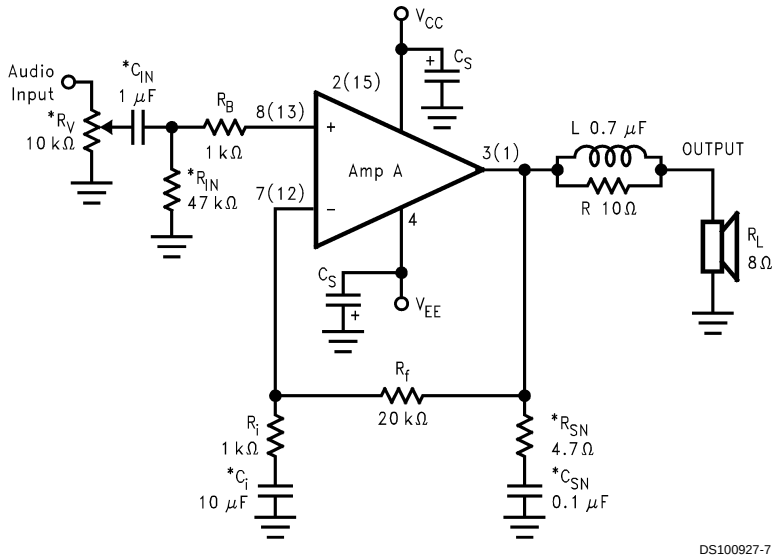
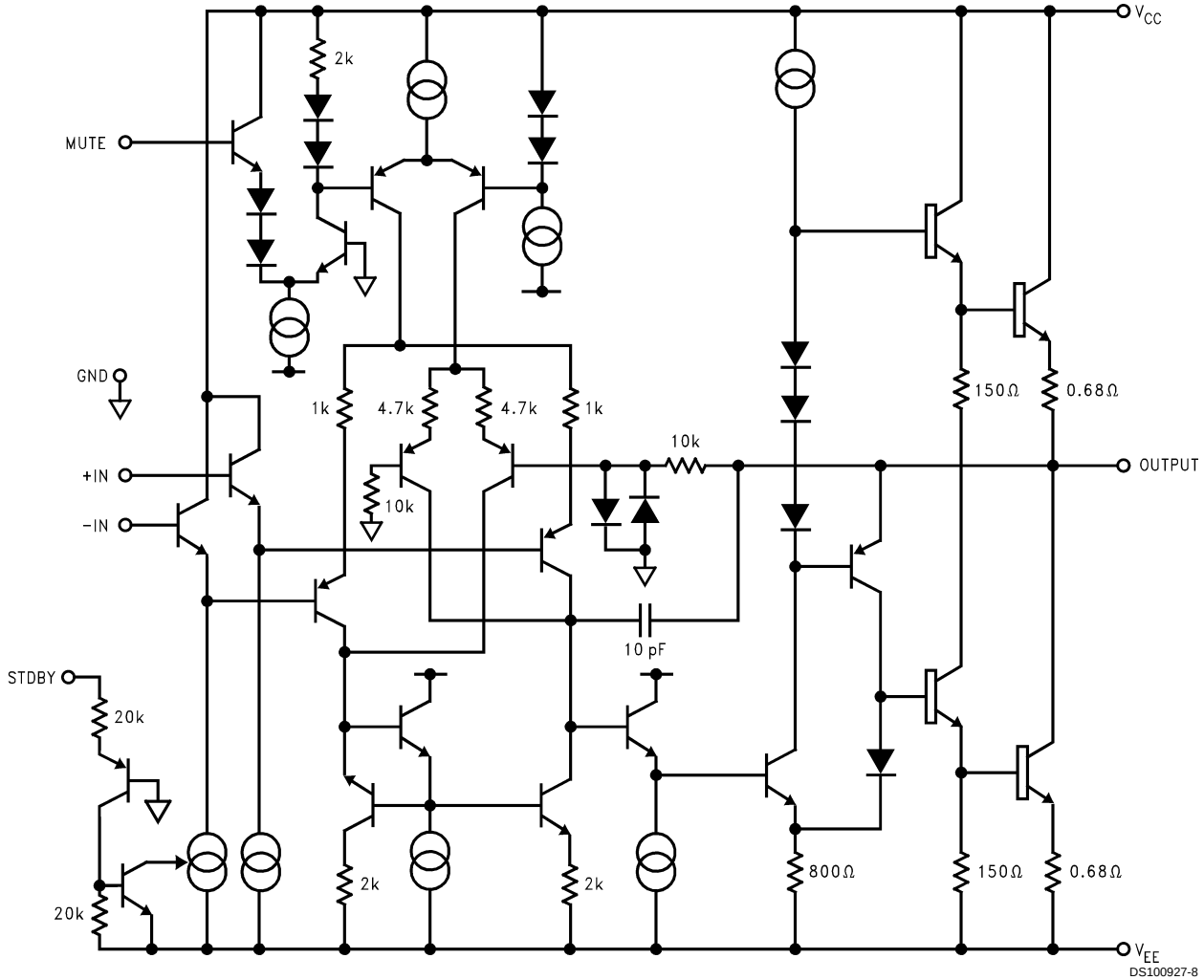


FIGURE 4. Special Audio Amplifier Application Circuit

Equivalent Schematic (excluding active protection circuitry)

LM4765 (One Channel Only)



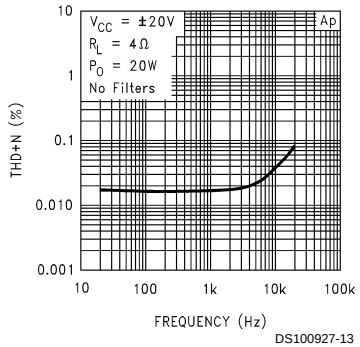
External Components Description

Components		Functional Description
1	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power down of the system due to the low input impedance of the circuitry when the undervoltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
2	R_i	Inverting input resistance to provide AC gain in conjunction with R_f.
3	R_f	Feedback resistance to provide AC gain in conjunction with R_i.
4	C_i (Note 13)	Feedback capacitor which ensures unity gain at DC. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
5	C_S	Provides power supply filtering and bypassing. Refer to the Supply Bypassing application section for proper placement and selection of bypass capacitors.
6	R_V (Note 13)	Acts as a volume control by setting the input voltage level.
7	R_{IN} (Note 13)	Sets the amplifier's input terminals DC bias point when C_{IN} is present in the circuit. Also works with C_{IN} to create a highpass filter at $f_C = 1/(2\pi R_{IN} C_{IN})$. Refer to *Figure 4*.
8	C_{IN} (Note 13)	Input capacitor which blocks the input signal's DC offsets from being passed onto the amplifier's inputs.
9	R_{SN} (Note 13)	Works with C_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities.
10	C_{SN} (Note 13)	Works with R_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities. The pole is set at $f_C = 1/(2\pi R_{SN} C_{SN})$. Refer to *Figure 4*.
11 12	L (Note 13) R (Note 13)	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load. Refer to *Figure 4*.
13	R_A	Provides DC voltage biasing for the transistor Q1 in single supply operation.
14	C_A	Provides bias filtering for single supply operation.
15	R_{INP} (Note 13)	Limits the voltage difference between the amplifier's inputs for single supply operation. Refer to the **Clicks and Pops** application section for a more detailed explanation of the function of R_{INP}.
16	R_{BI}	Provides input bias current for single supply operation. Refer to the **Clicks and Pops** application section for a more detailed explanation of the function of R_{BI}.
17	R_E	Establishes a fixed DC current for the transistor Q1 in single supply operation. This resistor stabilizes the half-supply point along with C_A.

Note 13: Optional components dependent upon specific design requirements.

Typical Performance Characteristics

THD + N vs Frequency



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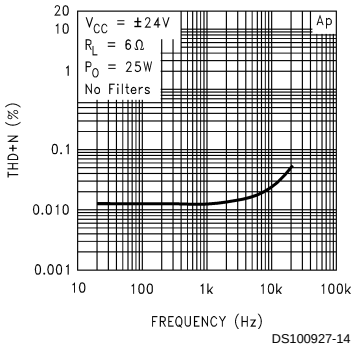
THD + N vs Frequency



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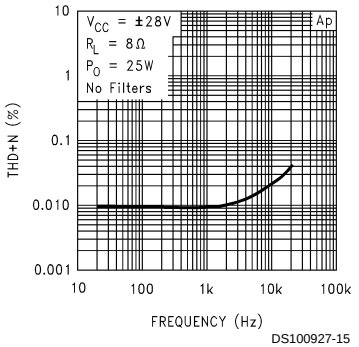
THD + N vs Frequency



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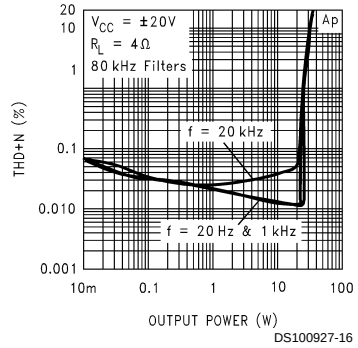
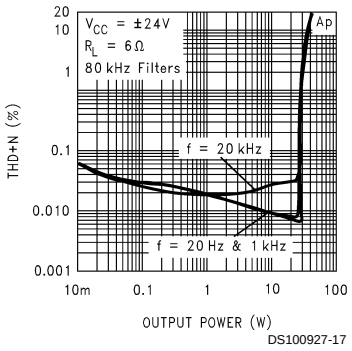
Typical Performance Characteristics (Continued)

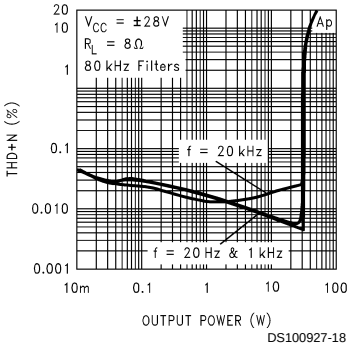
THD + N vs Output Power



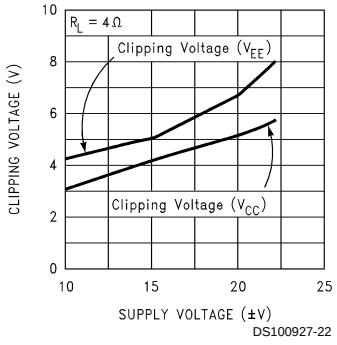
THD + N vs Output Power



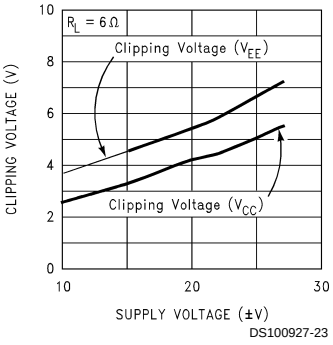
THD + N vs Output Power



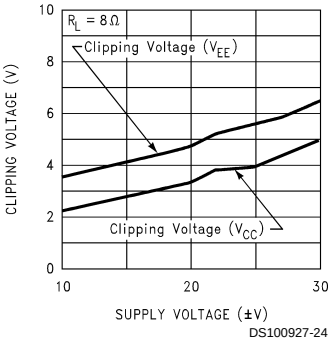
Clipping Voltage vs Supply Voltage



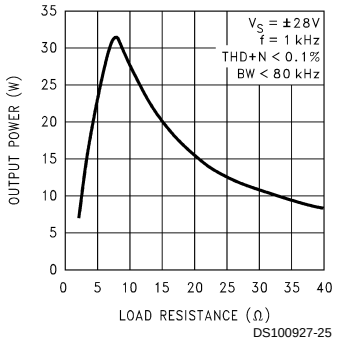
Clipping Voltage vs Supply Voltage



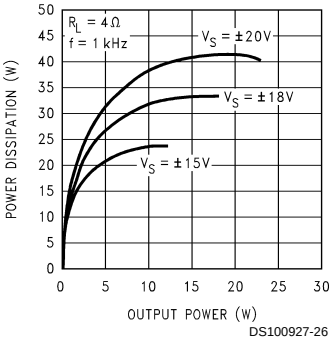
Clipping Voltage vs Supply Voltage



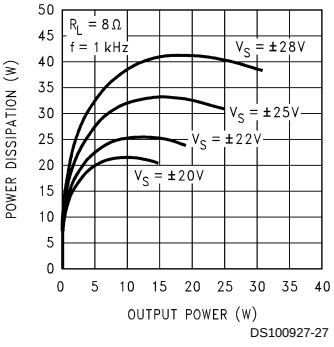
Output Power vs Load Resistance



Power Dissipation vs Output Power

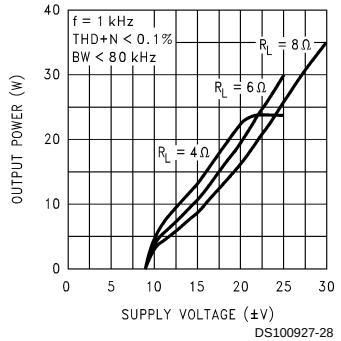


Power Dissipation vs Output Power



Typical Performance Characteristics (Continued)

Output Power vs Supply Voltage



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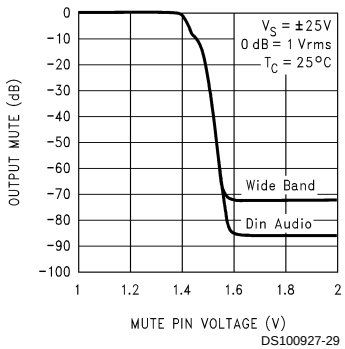
Output Mute vs Mute Pin Voltage



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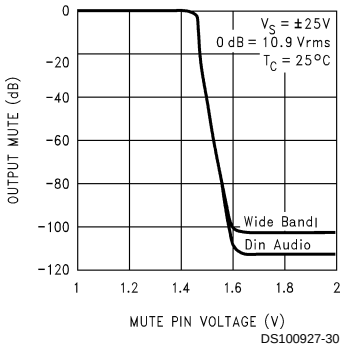
Output Mute vs Mute Pin Voltage



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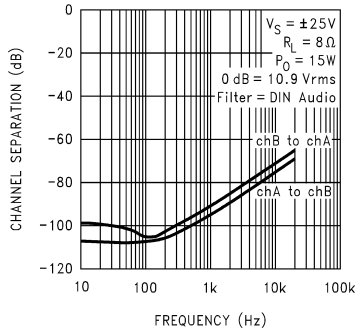
Channel Separation vs Frequency



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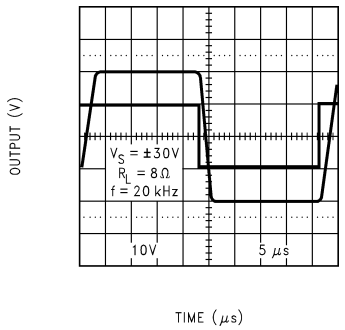
Pulse Response



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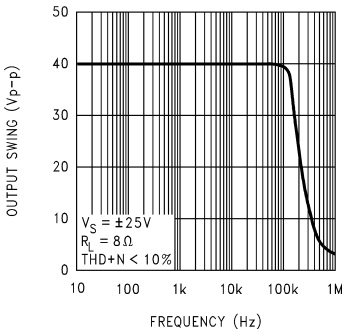
Large Signal Response



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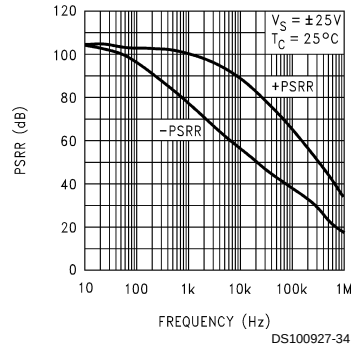
Power Supply Rejection Ratio



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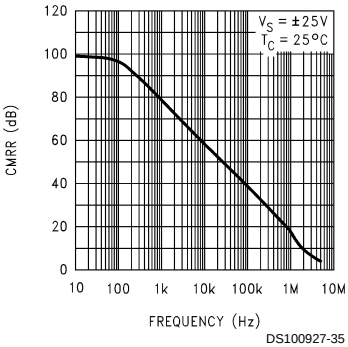
Common-Mode Rejection Ratio



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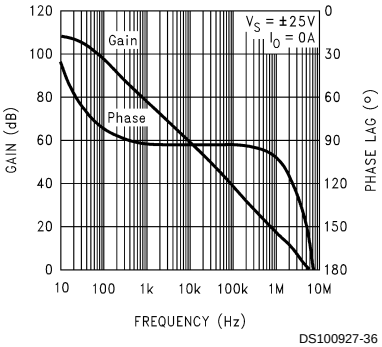
Open Loop Frequency Response



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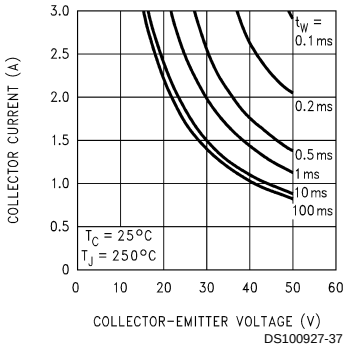
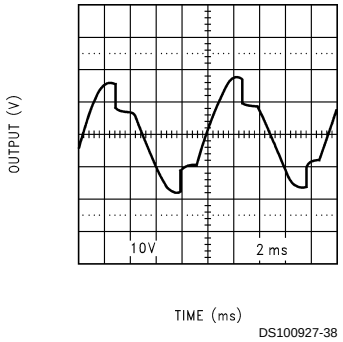
Typical Performance Characteristics (Continued)

Safe Area



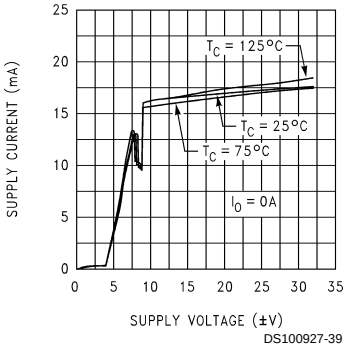
DS100927-37

SPiKe Protection Response



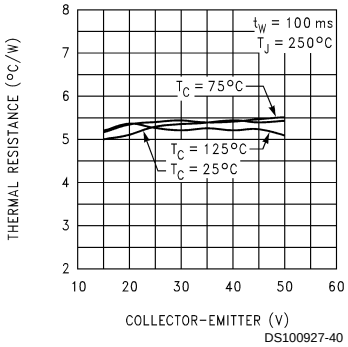
DS100927-38

Supply Current vs Supply Voltage



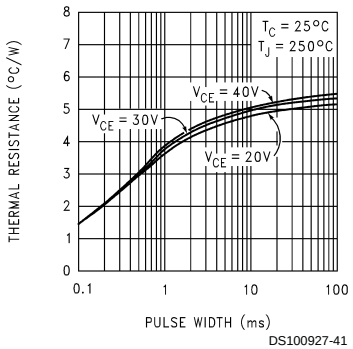
DS100927-39

Pulse Thermal Resistance



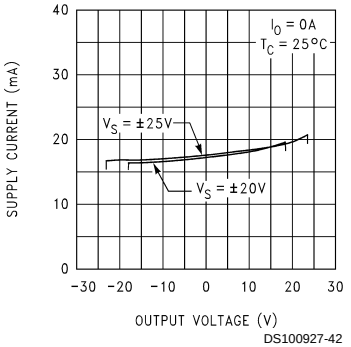
DS100927-40

Pulse Thermal Resistance



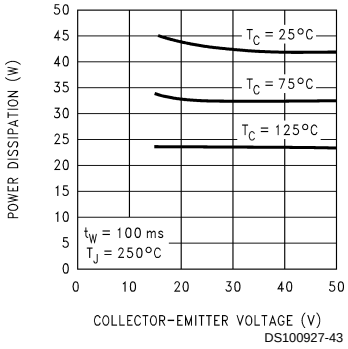
DS100927-41

Supply Current vs Output Voltage



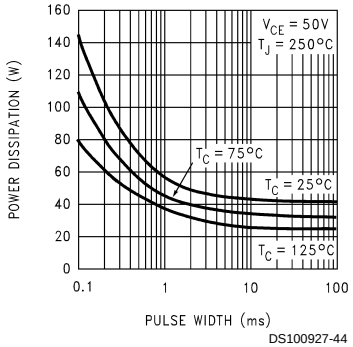
DS100927-42

Pulse Power Limit



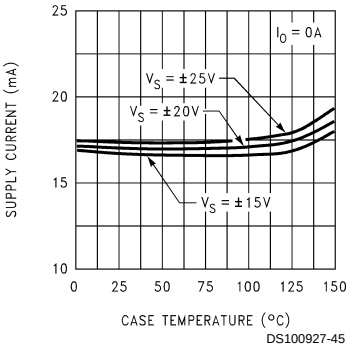
DS100927-43

Pulse Power Limit



DS100927-44

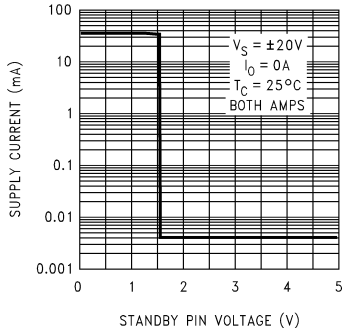
Supply Current vs Case Temperature



DS100927-45

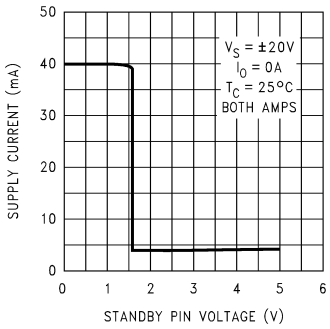
Typical Performance Characteristics (Continued)

Supply Current (I_{CC}) vs Standby Pin Voltage



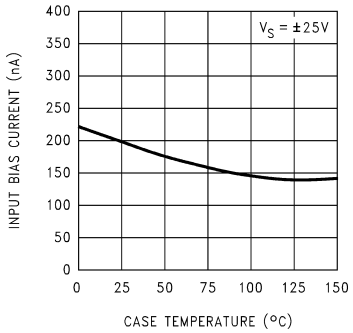
DS100927-46

Supply Current (I_{EE}) vs Standby Pin Voltage



DS100927-47

Input Bias Current vs Case Temperature



DS100927-48

Application Information

MUTE MODE

By placing a logic-high voltage on the mute pins, the signal going into the amplifiers will be muted. If the mute pins are left floating or connected to a logic-low voltage, the amplifiers will be in a non-muted state. There are two mute pins, one for each amplifier, so that one channel can be muted without muting the other if the application requires such a configuration. Refer to the **Typical Performance Characteristics** section for curves concerning Mute Attenuation vs Mute Pin Voltage.

STANDBY MODE

The standby mode of the LM4765 allows the user to drastically reduce power consumption when the amplifiers are idle. By placing a logic-high voltage on the standby pins, the amplifiers will go into Standby Mode. In this mode, the current drawn from the V_{CC} supply is typically less than 10 µA total for both amplifiers. The current drawn from the V_{EE} supply is typically 4.2 mA. Clearly, there is a significant reduction in idle power consumption when using the standby mode. There are two Standby pins, so that one channel can be put in standby mode without putting the other amplifier in standby if the application requires such flexibility. Refer to the **Typical Performance Characteristics** section for curves showing Supply Current vs. Standby Pin Voltage for both supplies.

UNDER-VOLTAGE PROTECTION

Upon system power-up, the under-voltage protection circuitry allows the power supplies and their corresponding capacitors to come up close to their full values before turning on the LM4765 such that no DC output spikes occur. Upon turn-off, the output of the LM4765 is brought to ground before the power supplies such that no transients occur at power-down.

OVER-VOLTAGE PROTECTION

The LM4765 contains over-voltage protection circuitry that limits the output current to approximately 3.5 Apk while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe PROTECTION

The LM4765 is protected from instantaneous peak-temperature stressing of the power transistor array. The Safe Operating graph in the **Typical Performance Characteristics** section shows the area of device operation where **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled. Please refer to AN-898 for more detailed information.

THERMAL PROTECTION

The LM4765 has a sophisticated thermal protection scheme to prevent long-term thermal stress of the device. When the temperature on the die reaches 165˚C, the LM4765 shuts down. It starts operating again when the die temperature drops to about 155˚C, but if the temperature again begins to rise, shutdown will occur again at 165˚C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165˚C and 155˚C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the **Determining the Correct Heat Sink** Section.

DETERMINING MAXIMUM POWER DISSIPATION

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation calculation may result in inadequate heat sinking causing thermal shutdown and thus limiting the output power.

Equation (1) exemplifies the theoretical maximum power dissipation point of each amplifier where V_{CC} is the total supply voltage.

$$P_{DMAX} = V_{CC}2/2\pi^2R_L \quad (1)$$

Thus by knowing the total supply voltage and rated output load, the maximum power dissipation point can be calculated. The package dissipation is twice the number which results from *Equation (1)* since there are two amplifiers in each LM4765. Refer to the graphs of Power Dissipation versus Output Power in the **Typical Performance Characteristics** section which show the actual full range of power dissipation not just the maximum theoretical point that results from *Equation (1)*.

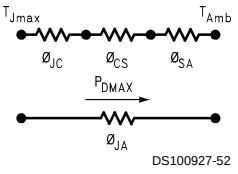
DETERMINING THE CORRECT HEAT SINK

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances.

The thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, θ_{JC}, θ_{CS}, and θ_{SA}. In addition, the thermal resistance, θ_{JC} (junction to case), of the LM4765 is 1˚C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2˚C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM4765 is equal to the following:

$$P_{DMAX} = (T_{JMAX}-T_{AMB})/\theta_{JA} \quad (2)$$

where T_{JMAX} = 150˚C, T_{AMB} is the system ambient temperature and $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$.



Once the maximum package power dissipation has been calculated using *Equation (1)*, the maximum thermal resistance, θ_{SA}, (heat sink to ambient) in ˚C/W for a heat sink can be calculated. This calculation is made using *Equation (3)* which is derived by solving for θ_{SA} in *Equation (2)*.

Application Information (Continued)

$$\theta_{SA} = [(T_{JMAX} - T_{AMB}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (3)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher than 25˚C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

SUPPLY BYPASSING

The LM4765 has excellent power supply rejection and does not require a regulated supply. However, to improve system performance as well as eliminate possible oscillations, the LM4765 should have its supply leads bypassed with low-inductance capacitors having short leads that are located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 µF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 µF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided, the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 µF or more.

BRIDGED AMPLIFIER APPLICATION

The LM4765 has two operational amplifiers internally, allowing for a few different amplifier configurations. One of these configurations is referred to as "bridged mode" and involves driving the load differentially through the LM4765's outputs. This configuration is shown in *Figure 2*. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a distinct advantage over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, theoretically four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. For each operational amplifier in a bridge configuration, the internal power dissipation will increase by a factor of two over the single ended dissipation. Thus, for an audio power amplifier such as the LM4765, which has two operational amplifiers in one package, the package dissipation will increase by a factor of four. To calculate the LM4765's maximum power dissipation point for a bridged load, multiply *Equation (1)* by a factor of four.

This value of P_{DMAX} can be used to calculate the correct size heat sink for a bridged amplifier application. Since the internal dissipation for a given power supply and load is increased by using bridged-mode, the heatsink's θ_{SA} will have to decrease accordingly as shown by *Equation (3)*. Refer to the section, **Determining the Correct Heat Sink,** for a more detailed discussion of proper heat sinking for a given application.

SINGLE-SUPPLY AMPLIFIER APPLICATION

The typical application of the LM4765 is a split supply amplifier. But as shown in *Figure 3*, the LM4765 can also be used in a single power supply configuration. This involves using some external components to create a half-supply bias which is used as the reference for the inputs and outputs. Thus, the signal will swing around half-supply much like it swings around ground in a split-supply application. Along with proper circuit biasing, a few other considerations must be accounted for to take advantage of all of the LM4765 functions.

The LM4765 possesses a mute and standby function with internal logic gates that are half-supply referenced. Thus, to enable either the Mute or Standby function, the voltage at these pins must be a minimum of 2.5V above half-supply. In single-supply systems, devices such as microprocessors and simple logic circuits used to control the mute and standby functions, are usually referenced to ground, not half-supply. Thus, to use these devices to control the logic circuitry of the LM4765, a "level shifter," like the one shown in *Figure 5*, must be employed. A level shifter is not needed in a split-supply configuration since ground is also half-supply.

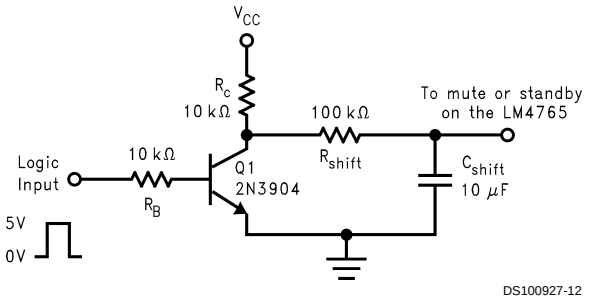


FIGURE 5. Level Shift Circuit

When the voltage at the Logic Input node is 0V, the 2N3904 is "off" and thus resistor R_c pulls up mute or standby input to the supply. This enables the mute or standby function. When the Logic Input is 5V, the 2N3904 is "on" and consequently, the voltage at the collector is essentially 0V. This will disable the mute or standby function, and thus the amplifier will be in its normal mode of operation. R_{shift}, along with C_{shift}, creates an RC time constant that reduces transients when the mute or standby functions are enabled or disabled. Additionally, R_{shift} limits the current supplied by the internal logic gates of the LM4765 which insures device reliability. Refer to the Mute Mode and Standby Mode sections in the **Application Information** section for a more detailed description of these functions.

CLICKS AND POPS

In the typical application of the LM4765 as a split-supply audio power amplifier, the IC exhibits excellent "click" and "pop" performance when utilizing the mute and standby modes. In addition, the device employs Under-Voltage Protection, which eliminates unwanted power-up and power-down transients. The basis for these functions are a stable and constant half-supply potential. In a split-supply application, ground is the stable half-supply potential. But in a single-supply application, the half-supply needs to charge up just like the supply rail, V_{CC}. This makes the task of attaining a clickless and popless turn-on more challenging. Any uneven charging of the amplifier inputs will result in output clicks and pops due to the differential input topology of the LM4765.

Application Information (Continued)

To achieve a transient free power-up and power-down, the voltage seen at the input terminals should be ideally the same. Such a signal will be common-mode in nature, and will be rejected by the LM4765. In *Figure 3*, the resistor R_{INP} serves to keep the inputs at the same potential by limiting the voltage difference possible between the two nodes. This should significantly reduce any type of turn-on pop, due to an uneven charging of the amplifier inputs. This charging is based on a specific application loading and thus, the system designer may need to adjust these values for optimal performance.

As shown in *Figure 3*, the resistors labeled R_{BI} help bias up the LM4765 off the half-supply node at the emitter of the 2N3904. But due to the input and output coupling capacitors in the circuit, along with the negative feedback, there are two different values of R_{BI}, namely 10 kΩ and 200 kΩ. These resistors bring up the inputs at the same rate resulting in a popless turn-on. Adjusting these resistors values slightly may reduce pops resulting from power supplies that ramp extremely quick or exhibit overshoot during system turn-on.

AUDIO POWER AMPLIFIER DESIGN

Design a 15W/8Ω Audio Amplifier

Given:

Power Output	15 Wrms
Load Impedance	8Ω
Input Level	1 Vrms(max)
Input Impedance	47 kΩ
Bandwidth	20 Hz−20 kHz ±0.25 dB

A designer must first determine the power supply requirements in terms of both voltage and current needed to obtain the specified output power. V_{OPEAK} can be determined from *Equation (4)* and I_{OPEAK} from *Equation (5)*.

$$V_{OPEAK} = \sqrt{(2R_LP_O)} \quad (4)$$

$$I_{OPEAK} = \sqrt{(2P_O)/R_L} \quad (5)$$

To determine the maximum supply voltage the following conditions must be considered. Add the dropout voltage to the peak output swing V_{OPEAK}, to get the supply rail at a current of I_{OPEAK}. The regulation of the supply determines the unloaded voltage which is usually about 15% higher. The supply voltage will also rise 10% during high line conditions. Therefore the maximum supply voltage is obtained from the following equation.

$$\text{Max supplies} \approx \pm (V_{OPEAK} + V_{OD})\ (1 + \text{regulation}) \quad (1.1)$$

For 15W of output power into an 8Ω load, the required V_{OPEAK} is 15.49V. A minimum supply rail of 20.5V results from adding V_{OPEAK} and V_{OD}. With regulation, the maximum supplies are ±26V and the required I_{OPEAK} is 1.94A from *Equation (5)*. It should be noted that for a dual 15W amplifier into an 8Ω load the I_{OPEAK} drawn from the supplies is twice 1.94 Apk or 3.88 Apk. At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD+N. In addition, the designer should verify that with the required power supply voltage and load impedance, that the required heatsink value θ_{SA} is feasible given system cost and size constraints. Once the heatsink issues have been addressed, the required gain can be determined from *Equation (6)*.

$$A_V \geq \sqrt{(P_OR_L)}/(V_{IN}) = V_{ORMS}/V_{INRMS} \quad (6)$$

From *Equation (6)*, the minimum A_V is: $A_V \geq 11$.

By selecting a gain of 21, and with a feedback resistor, R_f = 20 kΩ, the value of R_i follows from *Equation (7)*.

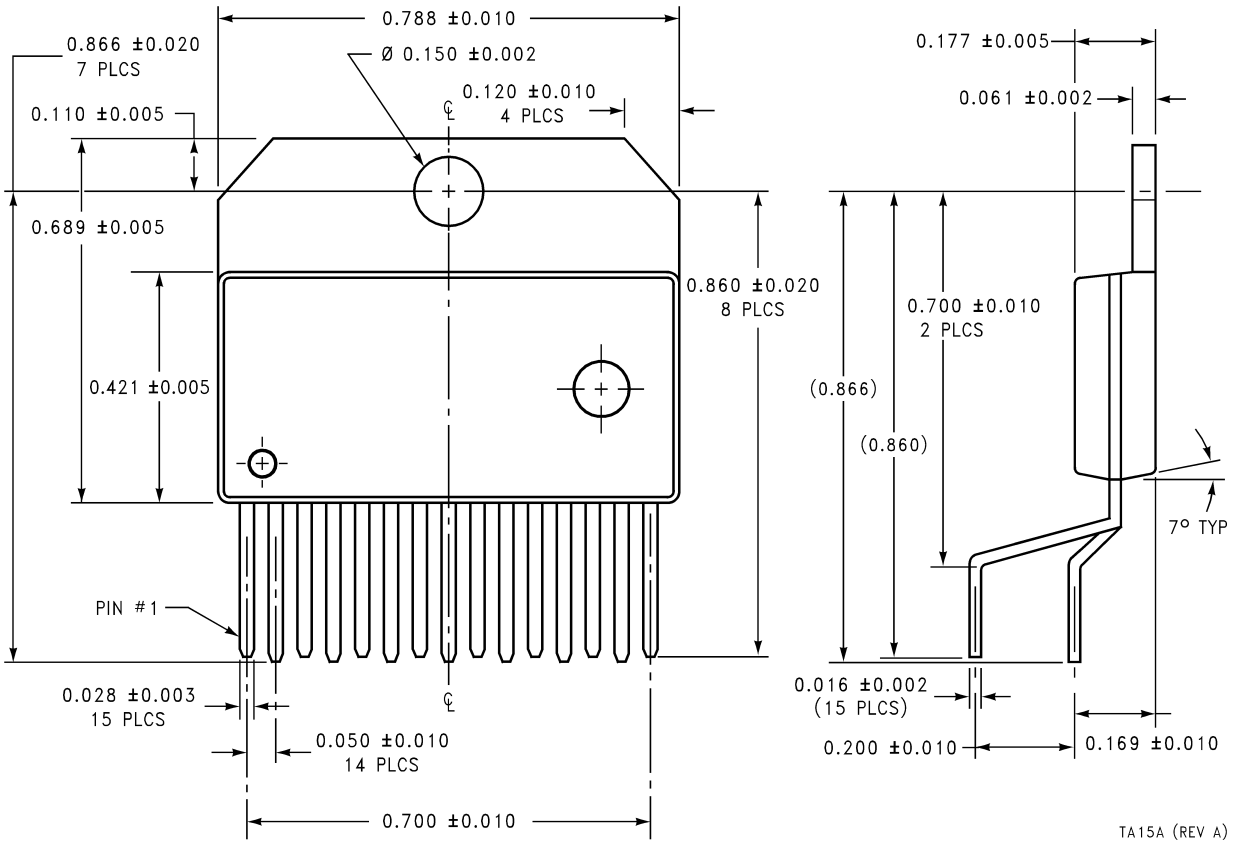
$$R_i = R_f\ (A_V - 1) \quad (7)$$

Thus with R_i = 1 kΩ a non-inverting gain of 21 will result. Since the desired input impedance was 47 kΩ, a value of 47 kΩ was selected for R_{IN}. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified. This fact results in a low and high frequency pole of 4 Hz and 100 kHz respectively. As stated in the **External Components** section, R_i in conjunction with C_i create a high-pass filter.

$$C_i \geq 1/(2\pi * 1\ k\Omega * 4\ Hz) = 39.8\ \mu F; \quad \text{use } 39\ \mu F.$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the gain, A_V. With a A_V = 21 and f_H = 100 kHz, the resulting GBWP is 2.1 MHz, which is less than the guaranteed minimum GBWP of the LM4765 of 5 MHz. This will ensure that the high frequency response of the amplifier will be no worse than 0.17 dB down at 20 kHz which is well within the bandwidth requirements of the design.

Physical Dimensions inches (millimeters) unless otherwise noted



Non-Isolated TO-220 15-Lead Package
Order Number LM4765T
NS Package Number TA15A

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